

What is claimed is:

1. An apparatus, comprising:
2 a converter converting an input optical signal to an original electrical signal;
3 an identification unit receiving said original electrical signal, generating a first signal corresponding to said original electrical signal delayed by a predetermined quantity of time, generating a second signal corresponding to said original electrical signal not delayed, comparing said first and second signals, forming a third signal in dependence upon said comparing of said first and second signals, detecting a bit rate in dependence upon said third signal;

a clock generator generating a reference clock signal in dependence upon said detected bit rate; and

a recovery unit recovering an input clock signal and data from said input optical signal in dependence upon said reference clock signal.

2. The apparatus of claim 1, said apparatus corresponding to an optical receiver receiving optical signals having a plurality of different bit rates.

3. The apparatus of claim 1, said bit rate of said input optical signal corresponding to a transmission rate.

1 4. The apparatus of claim 1, further comprising an amplifier amplifying said original
2 electrical signal received from said converter.

1 5. The apparatus of claim 4, said amplifier outputting said amplified electrical signal
2 to said identification unit.

1 6. The apparatus of claim 1, said converter corresponding to an optoelectric converter.

1 7. The apparatus of claim 1, said identification unit corresponding to a bit rate
identification unit.

1 8. The apparatus of claim 1, said comparing performed by said identification unit
corresponding to said identification unit performing an exclusive-OR logic operation upon said first
and second signals.

1 9. The apparatus of claim 8, said forming of said third signal performed by said
2 identification unit corresponding to said identification unit forming said third signal in dependence
3 upon said exclusive-OR logic operation performed upon said first and second signals.

1 10. The apparatus of claim 9, said identification unit comprising:

2 a first unit delaying said original electrical signal, performing said exclusive-OR operation
3 upon said first and second signals, and forming said third signal; and
4 a second unit filtering said third signal, detecting said bit rate in dependence upon a voltage
5 level of said filtered third signal.

11. The apparatus of claim 10, said filtering corresponding to low-pass filtering.

12. The apparatus of claim 10, said first unit corresponding to a bit rate identification
signal generator.

13. The apparatus of claim 10, said second unit corresponding to a bit rate deriving unit.

14. The apparatus of claim 10, said second unit comprising:

2 a filter filtering said third signal;

3 an analog-to-digital converter receiving said filtered third signal, converting said filtered third
4 signal from an analog signal to a digital signal; and

5 a determiner determining said bit rate in dependence upon said digital signal received from
6 said analog-to-digital converter.

1 15. The apparatus of claim 10, said first unit comprising:

2 a buffer unit receiving said original electrical signal, outputting two duplicate signals
3 substantially equivalent to said original electrical signal, said two duplicate signals corresponding
4 to a primary signal and a secondary signal;

5 a delay unit receiving said primary signal, delaying said primary signal by said predetermined
6 quantity of time, outputting said primary signal, said delayed primary signal corresponding to said
7 first signal; and

8 an operator unit performing said exclusive-OR logic operation upon said first and second
signals.

1 16. The apparatus of claim 1, said clock generator comprising a plurality of oscillators
2 generating clocking signals of different frequencies and selectively operating said oscillators to
3 generate said reference clock signal in dependence upon said bit rate detected by said identification
4 unit.

1 17. A method of operating a receiver which functions independently of a bit rate of a
2 received signal, comprising:

3 receiving an original signal;

4 generating a resultant signal by comparing a first signal and a second signal, said first signal
5 corresponding to said original signal delayed by a predetermined quantity of time, said second signal

6 corresponding to said original signal not delayed;
7 determining a bit rate of said original signal in dependence upon said resultant signal;
8 generating a reference clock signal in dependence upon said determined bit rate; and
9 recovering an input clock signal and data from said original signal in dependence upon said
10 reference clock signal.

1 18. The method of claim 17, said comparing of said first and second signals
2 corresponding to performing an exclusive-OR logic operation upon said first and second signals, said
resultant signal being generated as a result of said exclusive-OR logic operation.

1 19. The method of claim 18, further comprising:
2 said original signal corresponding to an input optical signal;
3 converting said input optical signal to an electrical signal;
4 outputting two duplicate signals substantially equivalent to said electrical signal, said two
5 duplicate signals corresponding to a primary signal and a secondary signal; and
6 delaying said primary signal by said predetermined quantity of time, outputting said primary
7 signal, said delayed primary signal corresponding to said first signal.

1 20. The method of claim 17, said first, second, and third signals corresponding to
2 electrical signals.

1 21. The method of claim 17, said method corresponding to receiving signals having a
2 plurality of different bit rates.

1 22. The method of claim 17, said original signal received corresponding to a plurality of
2 original signals received, said recovering of said input clock signal and data from said original signal
3 being performed for said plurality of original signals received, said plurality of original signals
4 received having a respective plurality of different bit rates.

1 23. The method of claim 17, said recovering of said input clock signal and data from said
original signal being performed for a plurality of original signals received, said plurality of original
signals received having a respective plurality of different bit rates.

1 24. The method of claim 17, said method corresponding to receiving optical signals
having a plurality of different bit rates.

1 25. The method of claim 17, further comprising:
2 receiving an input optical signal;
3 converting said input optical signal to an original electrical signal;
4 outputting two duplicate signals substantially equivalent to said original electrical signal, said

5 two duplicate signals corresponding to a primary signal and a secondary signal; and
6 delaying said primary signal by said predetermined quantity of time, outputting said primary
7 signal, said delayed primary signal corresponding to said first signal.

1 26. The method of claim 17, further comprising:

2 said receiving of said original signal being performed by an optoelectric converter, said
3 original signal being an optic signal, said optoelectric converter converting said original optic signal
4 to an electrical signal;

5 outputting two duplicate signals substantially equivalent to said electrical signal, said two
6 duplicate signals corresponding to a primary signal and a secondary signal, said outputting of said
7 two duplicate signals being performed by a buffer; and

8 delaying said primary signal by said predetermined quantity of time, outputting said primary
signal, said delayed primary signal corresponding to said first signal.

27. The method of claim 17, said generating of said reference clock signal being
2 performed by a clock generator, said clock generator comprising a plurality of oscillators generating
3 clocking signals of different frequencies and selectively operating said oscillators to generate said
4 reference clock signal in dependence upon said detected bit rate.

1 28. An apparatus, comprising:

- 2 a converter converting an input optical signal to an original electrical signal;
- 3 an identification unit receiving said original electrical signal, generating a first signal
- 4 corresponding to said original electrical signal delayed by a predetermined quantity of time, generating
- 5 a second signal corresponding to said original electrical signal not delayed, forming a third signal
- 6 by performing an exclusive-OR logic operation upon said first and second signals, detecting a bit
- 7 rate in dependence upon said third signal;
- 8 a clock generator generating a reference clock signal in dependence upon said detected bit
- 9 rate; and
- 10 a recovery unit recovering an input clock signal and data from said input optical signal in
- 11 dependence upon said reference clock signal.
- 12 29. The apparatus of claim 28, said clock generator comprising a plurality of oscillators
- 13 generating clocking signals of different frequencies and selectively operating said oscillators to
- 14 generate said reference clock signal in dependence upon said bit rate detected by said identification
- 15 unit.
- 16 30. The apparatus of claim 28, said input optical signal corresponding to a plurality of
- 17 input optical signals, said recovering of said input clock signal and data from said input optical
- 18 signal being performed for each of said plurality of input optical signals, said plurality of input
- 19 optical signals received having a plurality of different bit rates.

1 31. The apparatus of claim 30, said converter corresponding to an optoelectric converter.

1 32. The apparatus of claim 31, said identification unit corresponding to a bit rate
2 identification unit.

1 33. The apparatus of claim 32, said identification unit comprising:

2 a first unit delaying said original electrical signal, performing said exclusive-OR operation
upon said first and second signals, and forming said third signal; and

3 a second unit filtering said third signal, detecting said bit rate in dependence upon a voltage
level of said filtered third signal.

4 34. The apparatus of claim 33, said second unit comprising:

5 a filter filtering said third signal;

6 an analog-to-digital converter receiving said filtered third signal, converting said filtered third

signal from an analog signal to a digital signal; and

a determiner determining said bit rate in dependence upon said digital signal received from
said analog-to-digital converter.

1 35. The apparatus of claim 33, said first unit comprising:

2 a buffer unit receiving said original electrical signal, outputting two duplicate signals
3 substantially equivalent to said original electrical signal, said two duplicate signals corresponding
4 to a primary signal and a secondary signal;
5 a delay unit receiving said primary signal, delaying said primary signal by said predetermined
6 quantity of time, outputting said primary signal, said delayed primary signal corresponding to said
7 first signal; and
8 an operator unit performing said exclusive-OR logic operation upon said first and second
9 signals.

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36. The apparatus of claim 33, said clock generator comprising a plurality of oscillators generating clocking signals of different frequencies and selectively operating said oscillators to generate said reference clock signal in dependence upon said bit rate detected by said identification unit.

37. The apparatus of claim 33, said filtering corresponding to low-pass filtering.

38. The apparatus of claim 37, said second unit comprising:

2 a filter filtering said third signal;

3 an analog-to-digital converter receiving said filtered third signal, converting said filtered third
4 signal from an analog signal to a digital signal; and

5 a determiner determining said bit rate in dependence upon said digital signal received from
6 said analog-to-digital converter.

1 39. The apparatus of claim 38, said first unit comprising:

2 a buffer unit receiving said original electrical signal, outputting two duplicate signals
3 substantially equivalent to said original electrical signal, said two duplicate signals corresponding
4 to a primary signal and a secondary signal;

5 a delay unit receiving said primary signal, delaying said primary signal by said predetermined
6 quantity of time, outputting said primary signal, said delayed primary signal corresponding to said
7 first signal; and

8 an operator unit performing said exclusive-OR logic operation upon said first and second
9 signals.

10 40. The apparatus of claim 39, said clock generator comprising a plurality of oscillators
11 generating clocking signals of different frequencies and selectively operating said oscillators to
12 generate said reference clock signal in dependence upon said bit rate detected by said identification
13 unit.